UMP1

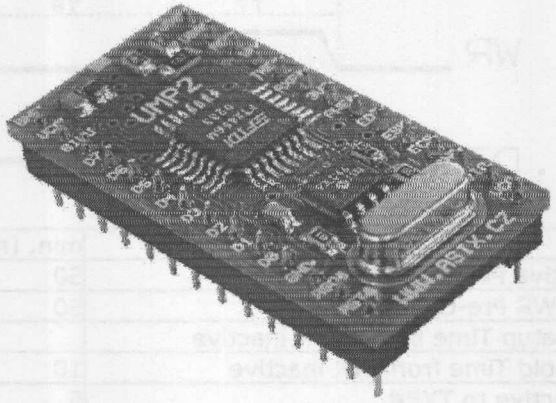
USB to 8-bit parallel FIFO
interface module

User's manual

ASIX®

1. UMP2

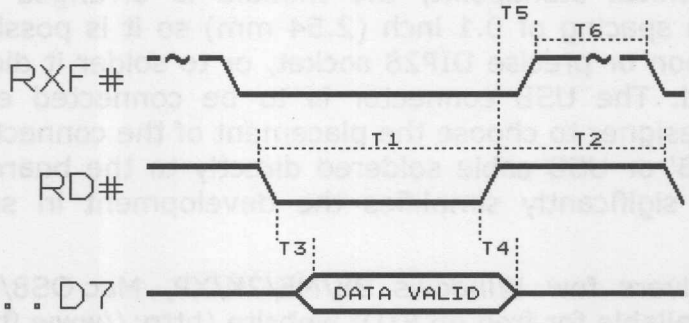
UMS1 is a module based on FT8U245AM integrated circuit manufactured by FTDI Ltd., which provides with easy to use USB connectivity to PC without any need of additional knowledge about USB itself.



2. USAGE

UMP1 is a USB to 8-bit bidirectional parallel FIFO interface with simple flow control.

2.1. FIFO read cycle

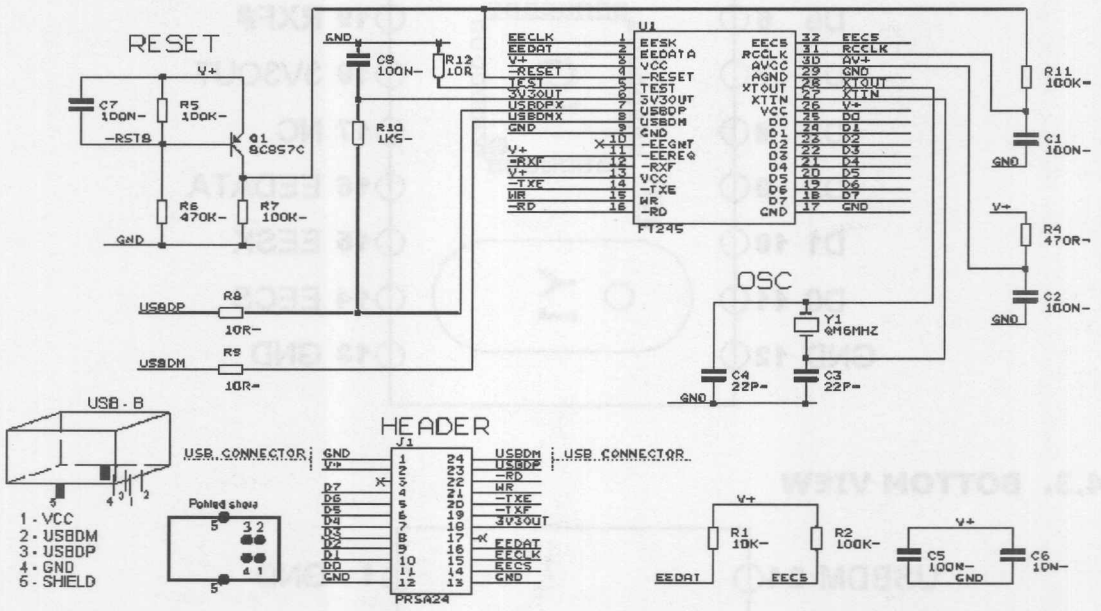


		min. [ns]	max. [ns]
T1	RD Active Pulse Width	50	
T2	RD to RD Pre-Charge Time	50	
T3	RD Active to Valid Data		30
T4	Valid Data Hold Time from RD inactive	10	
T5	RD Inactive to RXF#	5	25
T6	RXF# inactive after RD cycle	80	

- Supports USB 1.1 protocol, USB 2.0 compatible
- Support for OEM applications (VID and PID can be stored in external EEPROM memory)
- Drivers for Windows 98/2K/ME/XP, Mac OS8/OS9/OS X and Linux available for free
- DIP28 socket compatible, PCB mountable

4. TECHNICAL REFERENCE

4.1. SCHEMATICS



4.4. PIN DESCRIPTION

Pin	Label	FTDI	Typ	Description
1	GND	GND	PWR	Signal ground
2	VCC	VCC	PWR	Power supply +4.4 V to 5.25 V
3	NC		NC	Not connected
4	D7	D7	I/O	Bidirectional data bus, bit 7
5	D6	D6	I/O	Bidirectional data bus, bit 6
6	D5	D5	I/O	Bidirectional data bus, bit 5
7	D4	D4	I/O	Bidirectional data bus, bit 4
8	D3	D3	I/O	Bidirectional data bus, bit 3
9	D2	D2	I/O	Bidirectional data bus, bit 2
10	D1	D1	I/O	Bidirectional data bus, bit 1
11	D0	D0	I/O	Bidirectional data bus, bit 0
12	GND	GND	PWR	Signal ground
13	GND	GND	PWR	Signal ground
14	ECS	EECS	I/O	EEPROM enable – internal pull-up of 200 kOhm during reset.
15	ESK	EESK	OUT	EEPROM clock - high impedance during reset.
16	EDT	EEDATA	I/O	EEPROM data I/O - high impedance during reset.
17	NC		NC	Not connected
18	3V3	3V3OUT	OUT	3.3 V output from internal voltage regulator - this pin can source up to 5 mA.
19	RXF#	RXF#	OUT	Data ready, if this signal is log.0, the data may be read by 1-0-1 sequence on RD# pin. If the RXF# signal is log.1, the data is invalid.
20	TXE#	TXE#	IN	Transmit enabled, if this signal is log.0 the data may be written by 0-1-0 sequence on WR pin. If the TXE# signal is log.1, the buffer if full.
21	WR	WR	IN	Write signal – falling edge of this signal writes data to FTDI buffer.
22	RD#	RD#	IN	Read data – falling edge of this signal causes 1 byte of data to be read from FTDI buffer and sent to data pins.
23	USBDP	USBDP	I/O	USB data signal plus. It is necessary to connect resistor of 1.5 kOhm between USBDP and 3V3OUT or RSTOUT#.
24	USBDM	USBDM	I/O	USB data signal minus.

7. CONTACT

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